CLAIMS

1. A production process for producing a plurality of semiconductor devices on chip areas which are defined on a wafer, which production process comprises:

processing said wafer such that each of said chip areas is produced as a semi-finished semiconductor device by forming a first wiring-arrangement section on each of said chip areas;

subjecting said wafer to a provisional yield-rate test in which it is examined whether each of the semi-finished semiconductor devices on said wafer is acceptable or unacceptable; and

further processing said wafer such that each of said chip areas is produced as a finished semiconductor device by forming a second wiring-arrangement section on said first wiring-arrangement section when said wafer passes said provisional yield-rate test.

2. A production process as set forth in claim 1, wherein a yield-rate of acceptable semi-finished semiconductor devices is found in said provisional yield-rate test, and it is determined that said wafer has passed said provision yield-rate test when said yield-rate exceeds a predetermined permissible rate.

3. A production process as set forth in claim 1, wherein said first wiring-arrangement section is formed as a basic wiring-arrangement section to define plural kinds of basic electronic component formation areas in each of said chip areas, and said second wiring-arrangement section is formed as a customized wiring-arrangement section to establish electrical interconnections among said basic electrical component formation areas in accordance with a customer's request.

4. A production process as set forth in claim 1, wherein said basic wiring-arrangement section has a plurality of electrode pads formed on an uppermost surface thereof, for carrying out said provisional yield-rate test.

5. A production process as set forth in claim 1, further comprising:

subjecting said wafer to a genuine yield-rate test in which it is examined whether each of the finished semiconductor devices on said wafer is acceptable or unacceptable to thereby find a yield-rate of acceptable finished semiconductor devices; and

finally processing said wafer when said wafer passes said genuine yield-rate test.

6. A production process as set forth in claim 5, wherein a yield-rate of acceptable finished semiconductor devices is found in said genuine yield-rate test, and it is determined that said wafer has passed said genuine yield-rate test when said yield-rate exceeds a predetermined permissible rate.

7. A production process as set forth in claim 5, wherein said customized wiring-arrangement section has a plurality of electrode pads formed on an uppermost surface thereof, and said genuine yield-rate test is carried out, using the electrode pads of said customized wiring-arrangement section.

8. A production process as set forth in claim 7, wherein said basic wiring-arrangement section is formed as a multi-layered wiring-arrangement section composed of at least two metal circuit pattern layers and at least one insulation layer alternately laminated on each of said chip areas, and said customized wiring-arrangement section is formed as a multi-layered wiring-arrangement section composed of at least two metal circuit pattern layers and at least one insulation layer alternately laminated on said basic wiring-arrangement section.

9. A plurality of semi-finished semiconductor devices formed on chip areas defined on a wafer, which comprises:

a wiring-arrangement section formed on each of said chip areas; and

a plurality of electrode pads formed on an uppermost surface of said wiring-arrangement section, said electrode pads being only used to examine whether or not there is a defect in said wiring-arrangement section.

10. A plurality of semi-finished semiconductor devices as set forth in claim 9, wherein said wiring-arrangement section is defined as a first wiring-arrangement section, and each of said chip areas is produced as a finished semiconductor device by forming a second wiring-arrangement section on said first wiring-arrangement section.

11. A plurality of semi-finished semiconductor devices as set forth in claim 10, wherein said first wiring-arrangement section is formed as a basic wiring-arrangement section to define plural kinds of basic electronic component formation areas in each of said chip areas, and said second wiring-arrangement section is formed as a customized wiring-arrangement section to establish electrical interconnections among said basic electrical component formation areas in accordance with a customer's request.

12. A plurality of finished semiconductor devices formed on chip areas defined on a wafer, which comprises:

a first wiring-arrangement section formed on each of said chip areas;

a plurality of electrode pads formed on an uppermost surface of said first wiring-arrangement section, said electrode pads being only used to examine whether or not there is a defect in said first wiring-arrangement section;

a second wiring-arrangement section formed on said

first wiring-arrangement section; and

a plurality of electrode pads formed on an uppermost surface of said second wiring-arrangement section, said electrode pads being utilized to examine whether or not there is a defect in second wiring-arrangement section.

13. A plurality of finished semiconductor devices as set forth in claim 12, wherein said first wiring-arrangement section is formed as a basic wiring-arrangement section to define plural kinds of basic electronic component formation areas in each of said chip areas, and said second wiring-arrangement section is formed as a customized wiring-arrangement section to establish electrical interconnections among said basic electrical component formation areas in accordance with a customer's request.

14. A semiconductor device comprising:

a chip base;

a first wiring-arrangement section formed on said chip base;

a plurality of electrode pads formed on an uppermost surface of said first wiring-arrangement section; and

a second wiring-arrangement section formed on said first wiring-arrangement section,

wherein said plurality of electrode pads are left on the uppermost surface of said first wiring-arrangement section which has been examined, using said electrode pads, to determine whether or not there are defects in said first wiring-arrangement section.

15. A semiconductor device as set forth in claim 14, wherein said first wiring-arrangement section is formed as a basic wiring-arrangement section to define plural kinds of basic electronic component formation areas in each of said chip areas, and said second wiring-arrangement section is formed as a customized wiring-arrangement section to

establish electrical interconnections among said basic electrical component formation areas in accordance with a customer's request.

16. A provisional yield-rate test system for testing a wafer having a plurality of semi-finished semiconductor devices formed on each of chip areas defined on said wafer, which comprises:

an examination system that examines whether each of said semi-finished semiconductor devices is acceptable or unacceptable;

a yield-rate calculation system that calculates a yield-rate of acceptable semi-finished semiconductor devices based on the results of examination obtained by said examination system; and

a yield-rate evaluation system that evaluates the calculated yield-rate to determine whether or not the wafer should be further processed.

17. A provisional yield-rate test system as set forth in claim 16, further comprising a wafer identification system that identifies the wafer to be tested.

18. A provisional yield-rate test system as set forth in claim 16, further comprising a storage system that stores the results of examination obtained by said examination system.

19. A provisional yield-rate test system as set forth in claim 18, wherein the results of examination obtained by said examination system are stored on a storage medium as a chip table having a plurality of flag data corresponding to the chip areas on the wafer.

20. A genuine yield-rate test system for testing a wafer having a plurality of finished semiconductor devices formed on each of chip areas defined on said wafer, each of the finished semiconductor devices being formed as a semi-finished semiconductor device by forming a first

wiring-arrangement section, and being then completed by forming a second wiring-arrangement section on said first wiring-arrangement section, said genuine yield-rate test system comprising:

a storage medium that stores results of examination in which it has been examined whether each of said semi-finished semiconductor devices is acceptable or unacceptable;

a determination system that determines whether each of said semi-finished semiconductor devices has been acceptable or unacceptable;

an examination system that examines whether each of said finished semiconductor devices is acceptable or unacceptable only when it is determined by said determination system that a corresponding semi-finished semiconductor device has been acceptable;

a yield-rate calculation system that calculates a yield-rate of acceptable finished semiconductor devices based on the results of examination obtained by said examination system; and

a yield-rate evaluation system that evaluates the calculated yield-rate to determine whether or not the wafer should be further processed.

21. A genuine yield-rate test system as set forth in claim 20, further comprising a wafer identification system that identifies the wafer to be tested.

22. A genuine yield-rate test system as set forth in claim 20, further comprising a storage system that stores the results of examination obtained by said examination system.

23. A genuine yield-rate test system as set forth in claim 22, wherein the results of examination obtained by said examination system are stored on a storage medium as a chip table having a plurality of flag data corresponding to the chip

areas on the wafer.